

CLAIMS

1. A method of manufacturing a memory cell comprising an electrically conductive word
5 line, an electrically conductive bit line, an electrical charge storage structure, a transistor
structure, and a bit line contact, said method comprising the steps of:

forming said charge storage structure so as to be conductively coupled to said bit
line via said transistor structure and said bit line contact;

10 forming said transistor structure so as to be conductively coupled to said word
line;

forming said bit line contact by forming a conductively doped polysilicon plug
within a contact hole bounded by insulating side walls; and

forming said doped polysilicon plug so as to define a substantially convex upper
plug surface profile in contact with said bit line.

15 2. A method of manufacturing a memory cell as claimed in claim 1 wherein said
insulating side walls are formed so as to comprise a first pair of opposing insulating side
walls along said first dimension and a second pair of opposing insulating side walls
along said second dimension.

20 3. A method of manufacturing a memory cell as claimed in claim 2 wherein said first
pair of opposing insulating side walls are formed so as to comprise respective layers of
insulating spacer material formed over a conductive line.

25 4. A method of manufacturing a memory cell as claimed in claim 2 wherein said second
pair of opposing insulating side walls are formed so as to comprise respective layers of
insulating material formed between respective contact holes.

30 5. A method of manufacturing a memory cell as claimed in claim 1 wherein said contact
hole is filled with said polysilicon plug to an uppermost extent of said insulating side
walls.

6. A method of manufacturing a memory cell comprising an electrically conductive word line, an electrically conductive bit line, an electrical charge storage structure, a transistor structure, and a bit line contact, said method comprising the steps of:

forming said charge storage structure so as to be conductively coupled to said bit line via said transistor structure and said bit line contact;

forming said transistor structure so as to be conductively coupled to said word line;

forming said bit line contact by forming a conductively doped polysilicon plug within a contact hole bounded by insulating side walls; and

forming said doped polysilicon plug by filling said contact hole to less than the uppermost extent of said insulating sidewalls with said conductively doped silicon plug such that said plug defines an upper plug surface profile substantially free of concavities in contact with said bit line.

7. A method of manufacturing a memory cell comprising an electrically conductive word line, an electrically conductive bit line, an electrical charge storage structure, a transistor structure, and a bit line contact, said method comprising the steps of:

forming said charge storage structure so as to be conductively coupled to said bit line via said transistor structure and said bit line contact;

forming said transistor structure so as to be conductively coupled to said word line;

forming said bit line contact by forming a conductively doped polysilicon plug within a contact hole bounded by insulating side walls; and

forming said doped polysilicon plug by partially filling said contact hole with said conductively doped silicon plug such that said plug defines an upper plug surface profile substantially free of concavities in contact with said bit line.

8. A method of manufacturing a memory cell comprising an electrically conductive word line, an electrically conductive bit line, an electrical charge storage structure, a transistor structure, and a bit line contact, said method comprising the steps of:

forming said charge storage structure so as to be conductively coupled to said bit line via said transistor structure and said bit line contact;

forming said transistor structure so as to be conductively coupled to said word line;

forming said bit line contact by forming a conductively doped polysilicon plug within a contact hole bounded by insulating side walls; and

forming said doped polysilicon plug by completely filling said contact hole with said conductively doped silicon plug such that said plug defines an upper plug surface profile substantially free of concavities in contact with said bit line.

9. A method of manufacturing a memory cell as claimed in claim 8, wherein said filling said contact hole with said conductively doped silicon plug is characterized by initial deposition and etch back of polysilicon in said contact hole and subsequent selective growth of conductively doped polysilicon in said contact hole.

10. A method of manufacturing a memory cell comprising an electrically conductive word line, an electrically conductive bit line, an electrical charge storage structure, a transistor structure, and a bit line contact, said method comprising the steps of:

forming said charge storage structure so as to be conductively coupled to said bit line via said transistor structure and said bit line contact;

forming said transistor structure so as to be conductively coupled to said word line;

forming said bit line contact by forming a conductively doped polysilicon plug within a contact hole bounded by insulating side walls; and

forming said doped polysilicon plug by partially filling said contact hole with said conductively doped silicon plug such that said plug defines a substantially convex upper plug surface profile in contact with said bit line.

11. A method of manufacturing a memory cell defined along first, second, and third orthogonal dimensions, said method comprising the steps of:

forming, along said first dimension, one-half of a bit line contact feature, one word line feature, one word line space feature, and one-half of a field poly line feature;

5 forming, along said second dimension, two one-half field oxide features and one active area feature such that said first and second dimensions define a $6F^2$ memory cell;

forming said bit line contact feature such that it is characterized by a contact hole bounded by insulating side walls;

10 filling said contact hole with a conductively doped polysilicon plug such that said plug defines a substantially convex upper plug surface profile;

forming a storage node such that it is characterized by a contact hole bounded by insulating side walls; and

15 filling said storage node contact hole with a conductively doped polysilicon plug such that said plug defines a substantially convex upper plug surface profile.

12. The method of claim 11 wherein said step of filling said contact hole comprises filling said contact hole with a conductive material, etching back said conductive material, and selectively growing doped polysilicon thereon.

20 13. The method of claim 11 wherein said step of filling said contact hole comprises partially filling said contact hole with a conductive material and selectively growing doped polysilicon thereon.

25 14. A method of manufacturing a memory cell comprising an electrically conductive word line, an electrically conductive bit line, an electrical charge storage structure, a transistor structure, and a bit line contact, said method comprising the steps of:

forming said charge storage structure so as to be conductively coupled to said bit line via said transistor structure and said bit line contact;

30 forming said transistor structure so as to be conductively coupled to said word line;

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forming said bit line contact by forming a conductively doped polysilicon plug within a contact hole bounded by insulating side walls;

forming said doped polysilicon plug so as to define a substantially convex upper plug surface profile in contact with said bit line;

5 forming a storage node such that it is characterized by a contact hole bounded by insulating side walls; and

filling said storage node contact hole with a conductively doped polysilicon plug such that said plug defines a substantially convex upper plug surface profile.

10 15. A method of manufacturing a memory cell defined along first, second, and third orthogonal dimensions, said method comprising the steps of:

forming, along said first dimension, one-half of a bit line contact feature, one word line feature, one word line space feature, and one-half of a field poly line feature;

15 forming, along said second dimension, two one-half field oxide features and one active area feature such that said first and second dimensions define a $6F^2$ memory cell;

forming said bit line contact feature such that it is characterized by a contact hole bounded by insulating side walls;

20 filling said bit line contact hole to less than the uppermost extent of said insulating sidewalls with a conductively doped polysilicon plug such that said plug defines an upper plug surface profile substantially free of concavities;

forming a storage node such that it is characterized by a contact hole bounded by insulating side walls; and

25 filling said storage node contact hole to less than the uppermost extent of said insulating sidewalls with a conductively doped polysilicon plug such that said plug defines an upper plug surface profile substantially free of concavities.

16. A method of manufacturing a memory cell defined along first, second, and third orthogonal dimensions, said method comprising the steps of:

30 forming, along said first dimension, one-half of a bit line contact feature, one word line feature, one word line space feature, and one-half of a field poly line feature;

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forming, along said second dimension, two one-half field oxide features and one active area feature such that said first and second dimensions define a $6F^2$ memory cell;

forming said bit line contact feature such that it is characterized by a contact hole bounded by insulating side walls;

partially filling said bit line contact hole with a conductively doped polysilicon plug such that said plug defines an upper plug surface profile substantially free of concavities;

forming a storage node such that it is characterized by a contact hole bounded by insulating side walls; and

partially filling said storage node contact hole with a conductively doped polysilicon plug such that said plug defines an upper plug surface profile substantially free of concavities.

17. A method of manufacturing a memory cell defined along first, second, and third orthogonal dimensions, said method comprising the steps of:

forming, along said first dimension, one-half of a bit line contact feature, one word line feature, one word line space feature, and one-half of a field poly line feature;

forming, along said second dimension, two one-half field oxide features and one active area feature such that said first and second dimensions define a $6F^2$ memory cell;

forming said bit line contact feature such that it is characterized by a contact hole bounded by insulating side walls;

completely filling said bit line contact hole with a conductively doped polysilicon plug such that said plug defines an upper plug surface profile substantially free of concavities;

forming a storage node such that it is characterized by a contact hole bounded by insulating side walls; and

completely filling said storage node contact hole with a conductively doped polysilicon plug such that said plug defines an upper plug surface profile substantially free of concavities.

18. A method of manufacturing a memory cell defined along first, second, and third orthogonal dimensions, said method comprising the steps of:

forming, along said first dimension, one-half of a bit line contact feature, one word line feature, one word line space feature, and one-half of a field poly line feature;

forming, along said second dimension, two one-half field oxide features and one active area feature such that said first and second dimensions define a $6F^2$ memory cell;

forming said bit line contact feature such that it is characterized by a contact hole bounded by insulating side walls;

partially filling said contact hole with a conductively doped polysilicon plug such that said plug defines a substantially convex upper plug surface profile;

forming a storage node such that it is characterized by a contact hole bounded by insulating side walls; and

partially filling said storage node contact hole with a conductively doped polysilicon plug such that said plug defines a substantially convex upper plug surface profile.